BT168GWF

SCR

Rev.03 - 28 February 2025 Product data sheet

1. General description

Planar passivated SCR with faster switching performance and sensitive gate in a SOT223 surface mounted plastic package. This SCR with enhanced commutation performance is also designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Fast commutation performance for higher frequency operation
- Full wave rectified AC applications
- Sensitive gate
- Direct triggering from microcontrollers, low power drivers and logic ICs

3. Applications

- Earth leakage circuit breakers (ELCB/GFI)
- Ignition circuits (gas appliances, small engines and HID lighting)

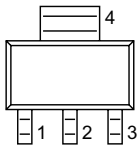
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values				Unit
Absolute maximum rating							
V_{RRM}	repetitive peak reverse voltage		600				V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 1	0.63				A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 2; Fig. 3	1				A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5	8				A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms	9				A
T_j	junction temperature		125				°C
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 10$ mA; $T_j = 25$ °C; Fig. 9		70	200	450	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402$ V; $T_j = 125$ °C; $R_{GK} = 1$ kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14		350	800	-	V/µs
		$V_{DM} = 402$ V; $T_j = 125$ °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 14		-	25	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
4	mb	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT168GWF	SOT223	BT168GWF, 115	Reel	1000	SOT223	03-Jun-2016

7. Marking

Table 4. Marking codes

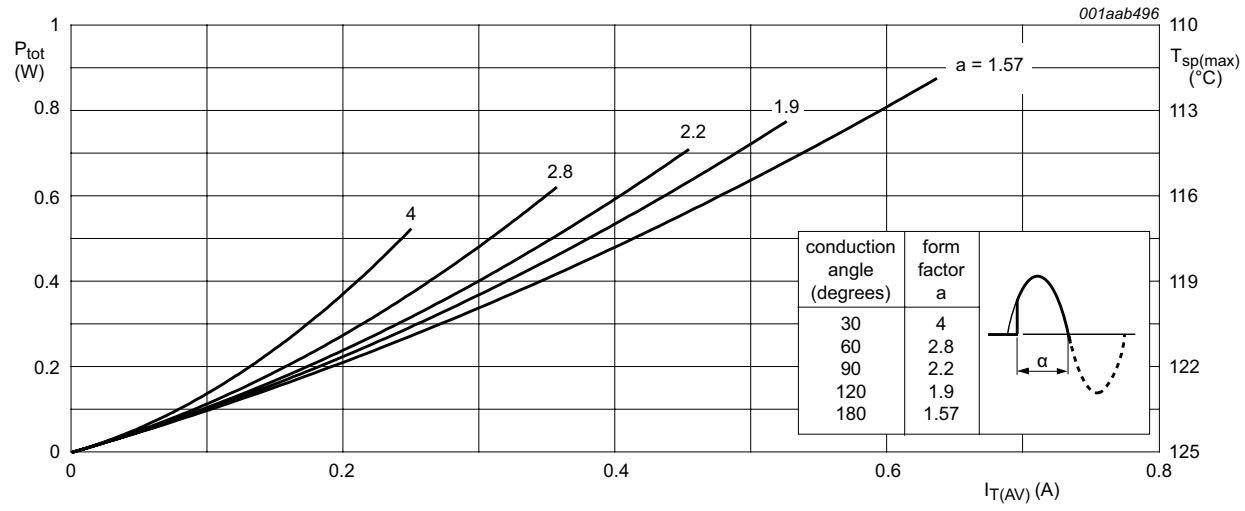
Type number	Marking codes	
	Assembly factory: d	Assembly factory: L
BT168GWF	Jdxxx 168GWF	JLxxx 168GWF

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		600	V
V_{RRM}	repetitive peak reverse voltage		600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 1	0.63	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 112$ °C; Fig. 2; Fig. 3	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5	8	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms	9	A
I^2t	I^2t for fusing	$t_P = 10$ ms; SIN	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 400$ mA	50	A/µs
I_{GM}	peak gate current		1	A
V_{RGM}	peak reverse gate voltage		5	V
P_{GM}	peak gate power		2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.1	W
T_{stg}	storage temperature		-40 to 150	°C
T_j	junction temperature		125	°C



a = form factor = $I_{T(RMS)} / I_{T(AV)}$

α = conduction angle

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

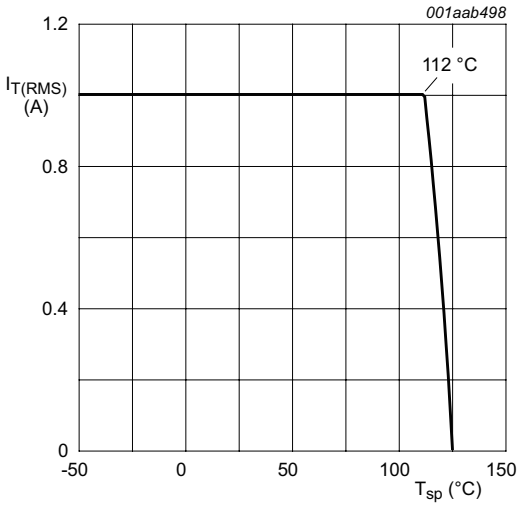
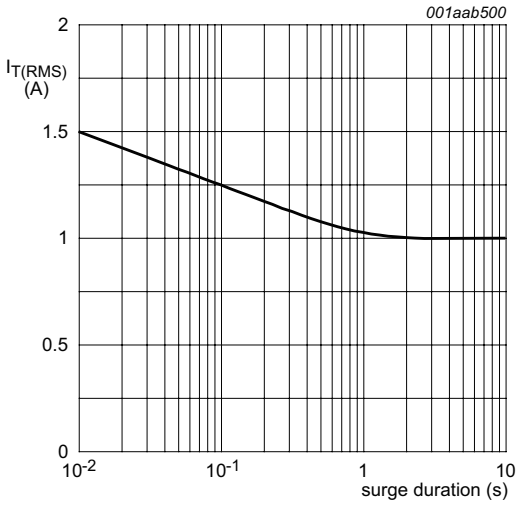
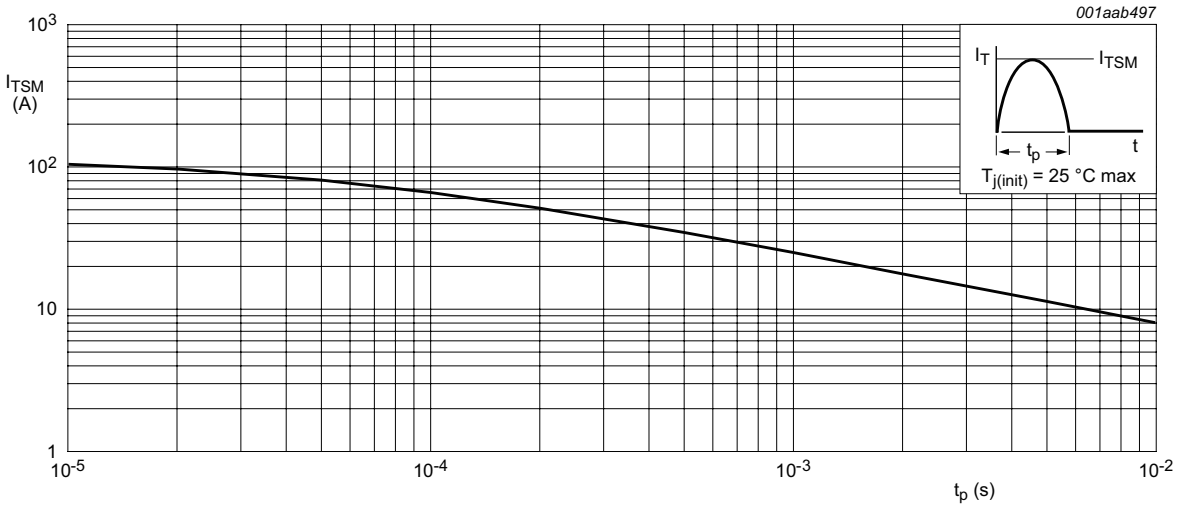


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values



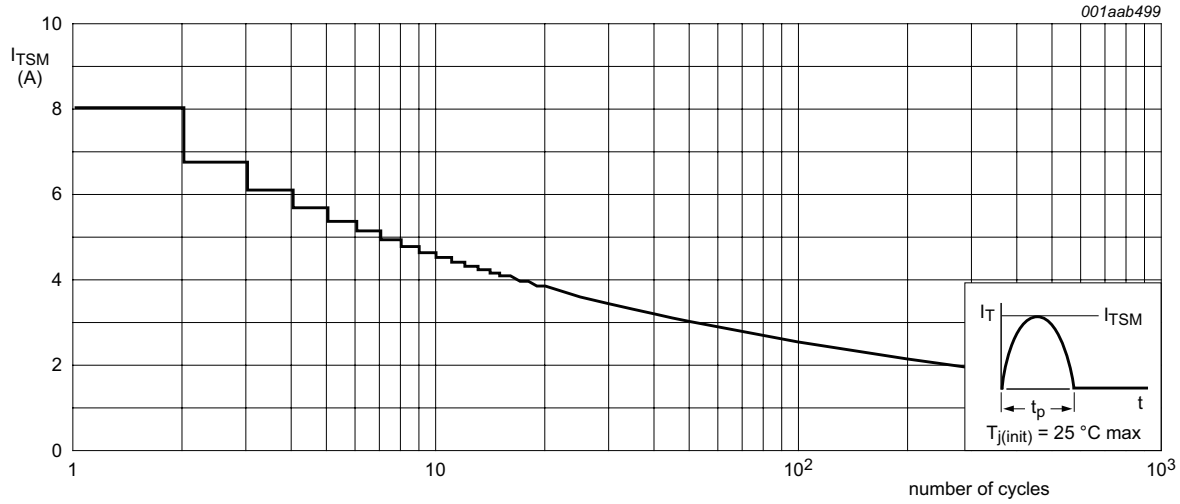
f = 50 Hz; T_{sp} = 112 °C

Fig. 3. RMS on-state current as a function of surge duration for sinusoidal currents



$t_p \leq 10$ ms

Fig. 4. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



f = 50 Hz

Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal currents cycles; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: minimum footprint; Fig. 7		-	156	-	K/W
		printed circuit board mounted: pad area; Fig. 8		-	70	-	K/W

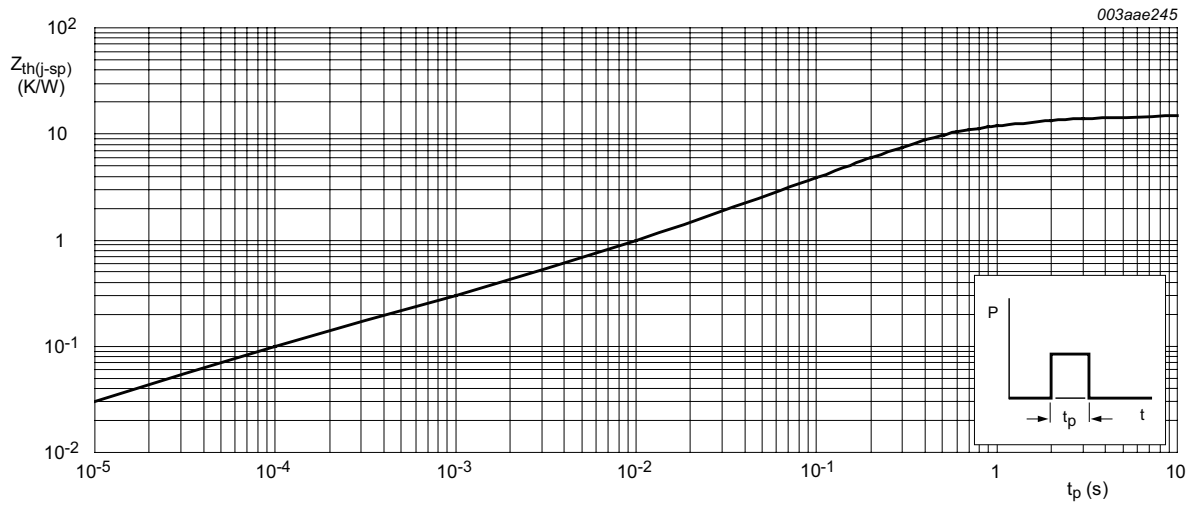
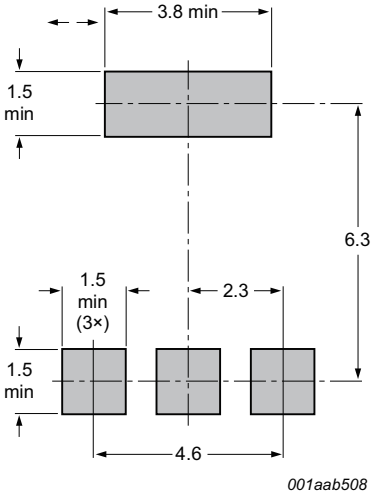
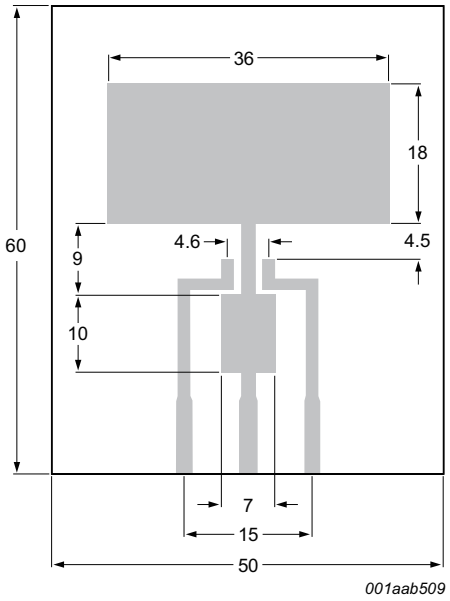


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 9		70	200	450	µA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 10		3	7.5	13	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 11		0.5	4.1	10	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 12		-	1.35	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 13		-	0.5	0.8	V
		V_D = 600 V; I_T = 10 mA; T_j = 125 °C		0.2	0.3	-	V
I_D	off-state current	V_D = 600 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	0.1	mA
I_R	reverse current	V_R = 600 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	0.1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK}=1kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14		350	800	-	V/µs
		V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 14		-	25	-	V/µs

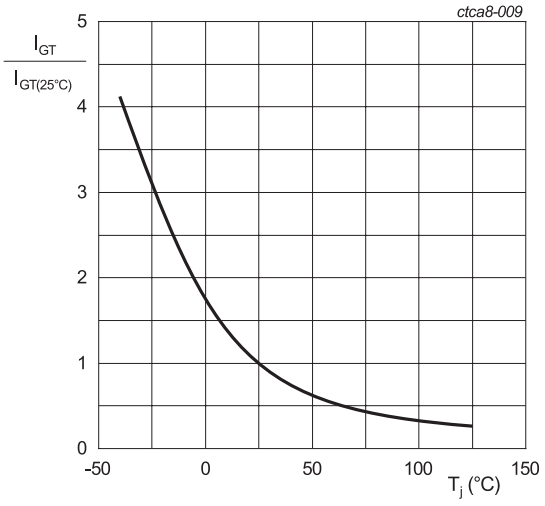


Fig. 9. Normalized gate trigger current as a function of junction temperature

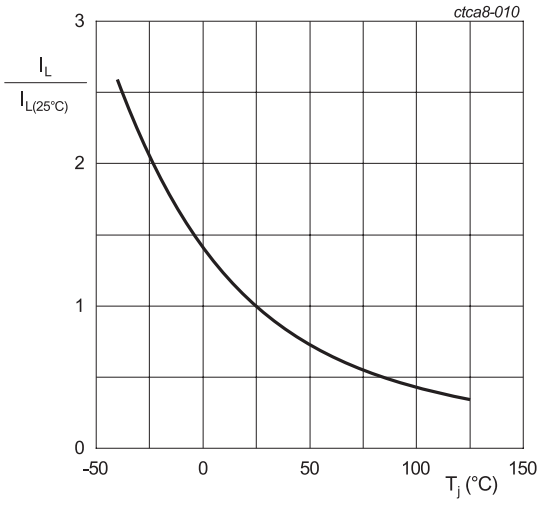


Fig. 10. Normalized latching current as a function of junction temperature

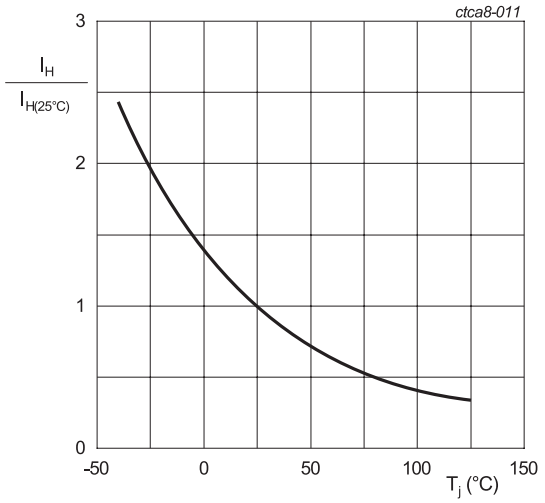
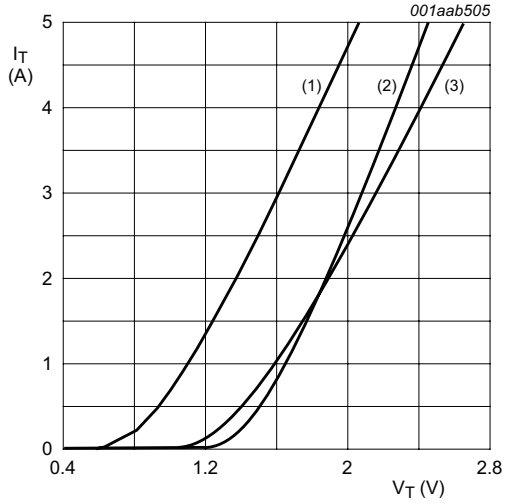


Fig. 11. Normalized holding current as a function of junction temperature



V_o = 1.0 V; R_s = 0.27 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

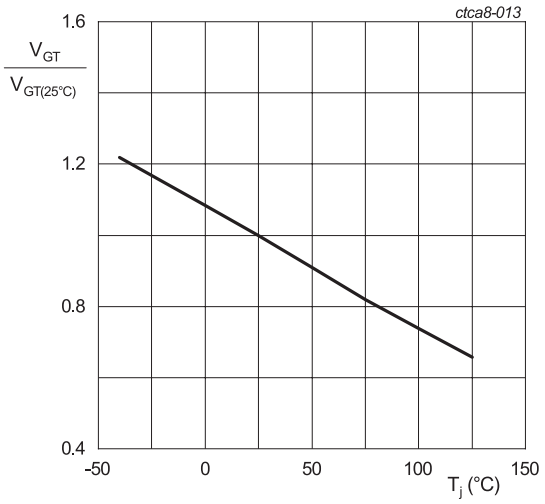
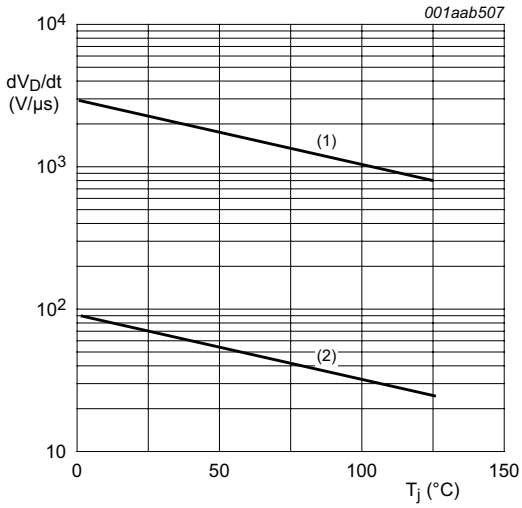


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

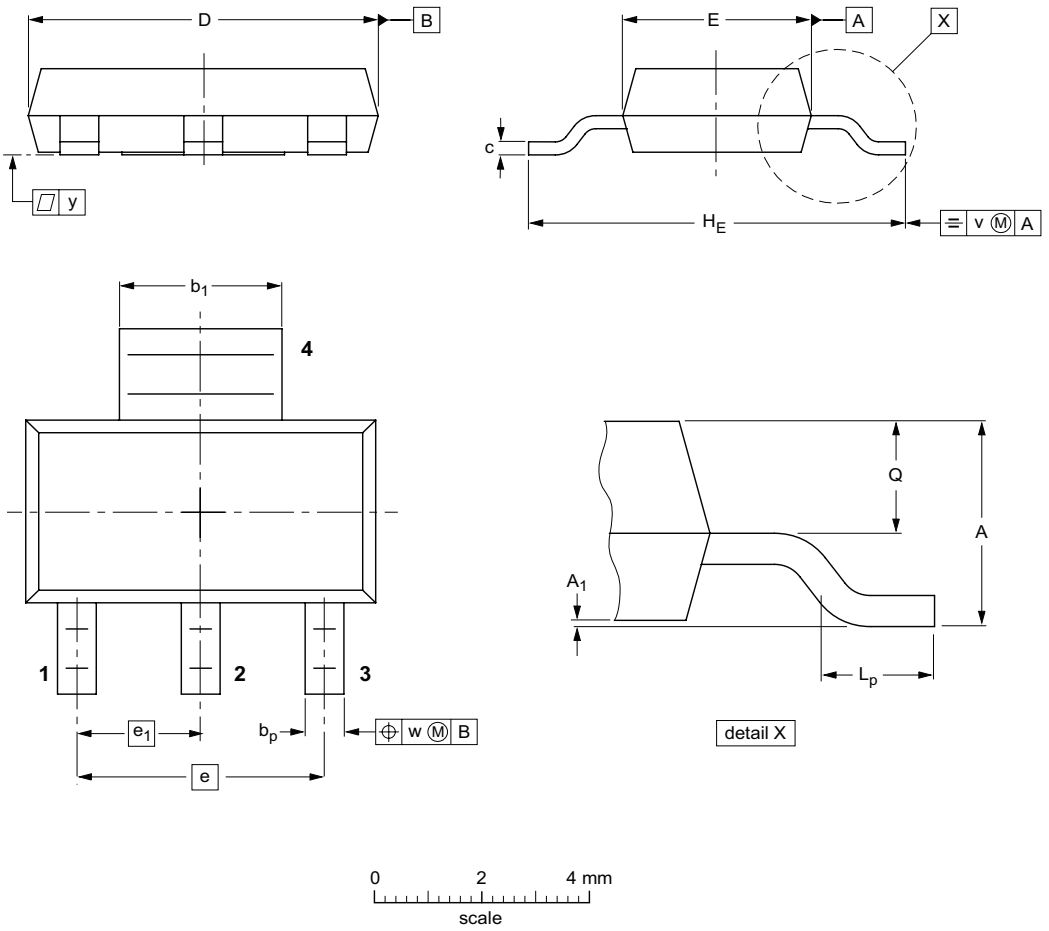


(1) R_{GK} = 1 kΩ;
(2) gate open circuit

Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

12. Soldering

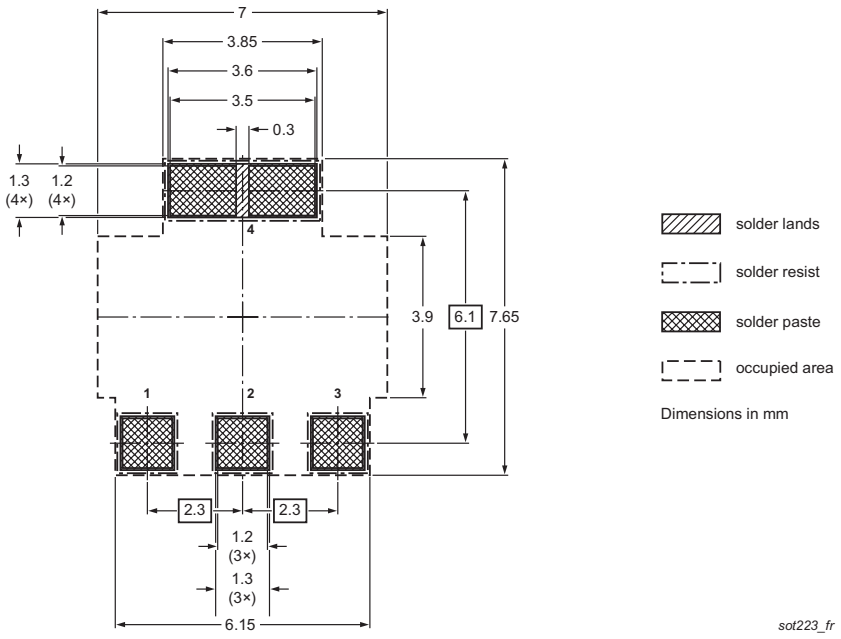


Fig. 15. Reflow soldering footprint for SOT223

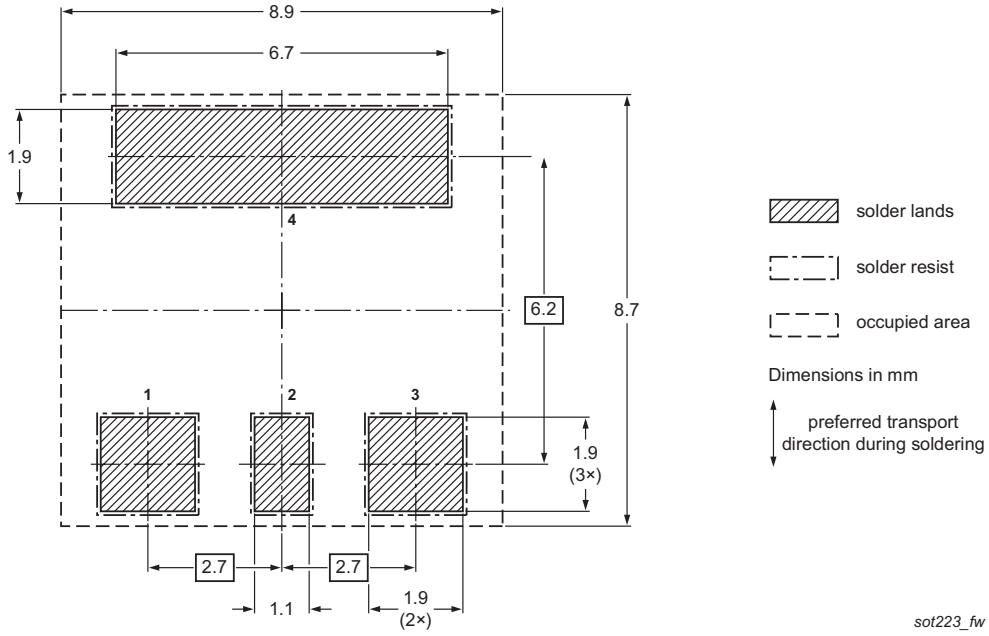


Fig. 16. Wave soldering foorprint for SOT223

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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14. Contents

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